Customer No.: 31561
Application No.: 10/064,266
Docket NO.:7554-US-PA

Claim Amendment

1. (currently amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate; and

forming a plurality of inter-metal dielectric layers on the substrate, wherein at least one ~~inter-metal dielectric layers~~ layer among ~~the plurality of~~ the inter-layer dielectrics and the inter-metal dielectric layers has a silicon carbide layer of about 100Å to about 1000Å thick formed thereon.

2. (previously canceled)

3. (original) The method of claim 1, wherein a thickness of the silicon carbide layer ranges from about 300Å to about 500Å.

4. (original)The method of claim 1, wherein forming the stacked gate structure comprises:

forming a composite dielectric layer on the substrate;

forming a gate conductive layer on the composite dielectric layer; and

patterning the gate conductive layer and the composite dielectric layer.

5. (original) The method of claim 4, wherein the composite dielectric layer comprises a tunnel oxide layer, a silicon nitride layer, and a silicon oxide layer.

6. (original) The method of claim 4, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

7. (original) The method of claim 4, wherein the method for forming the gate conductive layer comprises chemical vapor deposition (CVD).

8. (previously amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate; and

forming a silicon carbide layer of about 100Å to about 1000Å thick on the inter-layer dielectrics.

9. (previously canceled)

10. (original) The method of claim 8, wherein a thickness of the silicon carbide layer ranges from about 300Å to about 500Å.

11. (original) The method of claim 8, wherein forming the stacked gate structure comprises:

forming a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer on the substrate;

forming a gate conductive layer on the ONO composite layer; and

patterning the gate conductive layer and the ONO composite layer.

12. (original) The method of claim 11, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

13. (previously amended) A method for fabricating a flash memory, comprising the steps of:

forming a stacked gate structure and a source/drain on a substrate;

forming an inter-layer dielectrics on the substrate;

forming a contact in the inter-layer dielectrics;

forming a metal interconnection on the inter-layer dielectrics;

forming an inter-metal dielectrics on the substrate; and

forming a first silicon carbide layer of about 100Å to about 1000Å thick on the inter-metal dielectrics.

14. (previously canceled)

15. (currently canceled)

16. (currently canceled)

17. (original) The method of claim 13, wherein forming the stacked gate structure comprises:

forming a silicon oxide/silicon nitride/silicon oxide (ONO) composite layer on the substrate;

forming a gate conductive layer on the ONO composite layer; and

patterning the gate conductive layer and the ONO composite layer.

18. (original) The method of claim 17, wherein the gate conductive layer comprises a doped polysilicon layer and a metal silicide layer.

19. (original) The method of claim 18, wherein the metal silicide layer comprises a tungsten silicide layer.

20. (original) The method of claim 17, wherein the method for forming the gate conductive layer comprises chemical vapor deposition (CVD).

21(Reinstated-formerly claim 14) The method of claim 13, further comprising forming a second silicon carbide layer on the inter-layer dielectrics before the contact is formed in the inter-layer dielectrics.

22. (newly added) The method of claim 21, wherein a thickness of the second silicon carbide layer ranges from about 300 Å to about 500Å.